APPLICATIONS INFORMATION AN3

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SY6545
CRT Controller
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1.0 MPU/CRTC Memory Contention Techniques

The SY6545 CRT Controller is a device intended to provide for autonomous control of raster-scan display systems. A fully programmable unit, it permits convenient microprocessor programmability of most CRT display format parameters, such as, number of rows and columns, margin spacing, cursor position, scrolling, and more.

External to the SY6545, but fundamental to CRT systems, are two functions:

- Video Display Memory (RAM)
  - — Used to store character codes for each character position on the screen, usually ASCII
- Character Generator ROM
  - — Used to convert character codes from Video Display Memory into dot patterns for video generation

A unique requirement of the Video Display Memory is that it must be accessible by both the CRT Controller (to repetitively scan the video monitor) and the system MPU (to change the text or graphics displayed). The dual-access capability of the Video Display Memory presents systems problems which may be resolved in a variety of ways. Figure 1-1 illustrates a simple system block diagram showing an Address Contention Control function for this purpose.

Various Contention Schemes

As expected, there are several ways to accomplish the dual-access contention requirements of a CRT display system. Further, no one method is clearly superior, but each has its individual merits and drawbacks. The most common schemes for memory contention control are:

- MPU Priority
  - — In this approach, any microprocessor access of the memory overrides current CRT display accessing
- ϕ_1/ϕ_2 Interleave
  - — This method splits the system bus access, so that the MPU may access memory during ϕ_2 time and the CRTC, during ϕ_1.
- Vertical Blanking
  - — All MPU accesses are made during the vertical blanking time, when the screen is inactive.

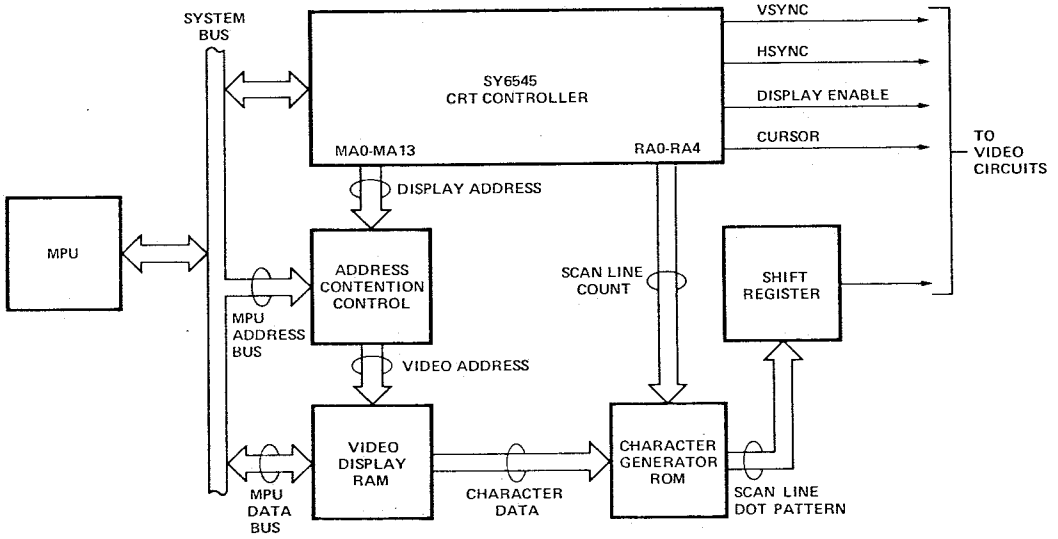

Figure 1-1. Video Display System Diagram

- Transparent Addressing — Blanking
  - This mode is unique to the SY6545 and permits MPU accesses to be made via the CRTC during horizontal and vertical blanking times
- Transparent Addressing — ϕ_1/ϕ_2 Interleave
  - Another unique SY6545 mode, this permits MPU accesses via the CRTC with ϕ_1/ϕ_2 bus splitting

The following sections outline each mode of operation.

1.2 MPU Priority

In this mode, the Address Contention Control block of Figure 1-1 is an address selector circuit. The arrangement of the selection is that the address lines from the CRTC (MA0-MA13) are normally gated to the Video Display RAM, except when MPU selects of the memory occur. The presence of a memory select (normally decoded from high-order MPU address lines) must cause the MPU address lines to immediately be gated to the Video Display RAM and the data bus of the MPU to be simultaneously gated, as well.

This technique has a significant advantage: it is easy to implement. However, it has a drawback, as well. When MPU accesses occur, the normal video display is disrupted and flashes occur on the screen. The flashes are not catastrophic, but are a nuisance and are not desirable in high-quality systems.

1.3 ϕ_1/ϕ_2 Interleave

The nature of the SY6500 (and, for that matter, the MC6800) system bus timing is such that each MPU cycle consists of two separate phases, ϕ_1 and ϕ_2, each of equal duration (although this need not be the case). The ϕ_1 portion is used by the MPU to generate address and R/W outputs. The ϕ_2 portion is used for all data bus transfers to and from the MPU. Fundamental to this approach, is the fact that the data bus is never used during ϕ_1 time, and, thus may be utilized for memory sharing. In this way, in the ϕ_1 portion of each clock cycle, the address lines from the CRTC must be gated to the memory and in the ϕ_2 portion, the MPU address lines are gated.

The result of this scheme is to overcome the screen flashing experienced in the MPU Priority method. Thus, a high-quality display results. This does not come free however. Since the memory is shared, the access time must be twice as fast. This is required since the memory now has only half a cycle to respond to accesses, whereas before, the entire cycle was utilized. One other constraint exists, as well. The character clock (CCLK) rate of the CRTC must be equal to, or an even multiple of, the MPU clock rate, so that proper memory access timing may be anticipated in the CRTC control timing.

1.4 Vertical Blanking

Utilization of the vertical blanking time of raster-scan displays overcomes disadvantages of both previous methods, but introduces its own drawback. To accommodate this technique, a facility must exist for the MPU to identify time intervals when the display is in its vertical blanking (retrace plus non-display margins) time. This can be of the form of a status bit (as in the SY6545) or an externally-generated MPU interrupt. In either case, the basic premise is for the MPU to perform all memory accesses during this vertical blanking time when the display is inactive and no flashing can occur. The address selection employs the simple MPU priority scheme described previously. As such, no special high-speed memory is required.

The only drawback is fairly significant. Since MPU access may only be done during vertical blanking times and since these interrupts only occur once for each frame (about 2-3 msec every 17 msec), significant time overhead may be encountered if the MPU is required to do a large number of accesses.

1.5 Transparent Addressing — Hor/Vert Blanking

Transparent Address modes are unique to the SY6545 and are described in great detail later in this document. A brief summary is given here to compare with the other methods presented.

Basically, Transparent Addressing with Hor/Vert Blanking accesses permits the MPU to access the Video Display RAM via the CRTC. The MPU must first load the desired memory address into the CRTC. Subsequently, the data to be stored is loaded into holding latches external to the CRTC — then, when the next horizontal or vertical blanking interval occurs (it doesn't matter which), the CRTC drives the address lines with the address loaded by the MPU and generates a strobe to cause the update (memory store) to occur. A "ready" bit in the SY6545 status register is used to indicate when this operation has transpired, so that the MPU may proceed with more memory updates, if desired. Figure 1-2 shows the system configuration for this mode.

Several advantages are apparent. First, the memory Address Contention circuits are not needed at all. This reduces parts count, but is offset somewhat by the requirement for the data holding latches. Second, no screen effects occur, since updates happen when the video is blanked. Third, it is not necessary for the MPU to be idle, waiting for vertical blanking, since horizontal blanking intervals are used, as well. Finally, slow memory may be utilized, because ϕ_1/ϕ_2 is not employed. The primary disadvantage is that somewhat more complex software control is required. Update addresses must be loaded into the CRTC and data into the holding latches for each update (although subsequent updates in consecutive memory locations are handled by the CRTC automatically incrementing the update address after each update). Further, the MPU must check the "ready" bit to perform successive updates.

1.6 Transparent Addressing — ϕ_1/ϕ_2 Interleave

This mode combines some features of Transparent Addressing with conventional memory sharing techniques. As expected, the Video Display RAM address lines are time-shared between ϕ_1 and ϕ_2 to permit immediate MPU access. In the ϕ_1 portion of the clock cycle, the address presented by the CRTC (MA0-MA13) is the address used for normal video display functions. During ϕ_2 time, however, the address is the internal Update Address Register. In this way, then, MPU writes to (or reads from) the Video Display RAM may be done directly, the only exception being for the MPU to have loaded the desired update address prior to the actual memory write or read.

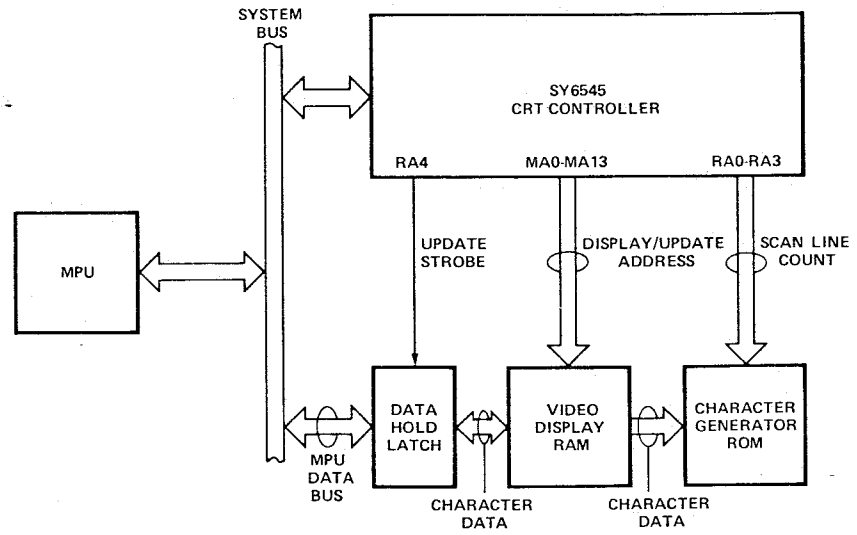

Figure 1-2. Transparent Addressing During Blanking Intervals

Thus, this mode is very similar to the normal ϕ_1/ϕ_2 Interleave method, except the address selection switching is built in to the CRTC. This is the primary advantage: the elimination of external address contention circuits. Two disadvantages are the need for fast memory and the programming requirement for the MPU to load update addresses before accessing memory.

1.7 Summary

Five methods for resolving display memory contention have been presented. Each has its own merits, as well as drawbacks. A summary is tabulated in Figure 1-3. It is hoped that this analysis helps to identify which technique is best for each particular system application.

Description of Method	Address Contention Circuits	Memory Speed	Software Requirements	Delay for Updates	Screen Effects
MPU Priority	Address Selector Switches	Slow	None	None	Flashing
ϕ_1/ϕ_2 Interleave	Address Selector Switches	Fast	None	None	None
Vertical Blanking	Address Selector Switches	Slow	Monitor Vertical Blank Status	Long (~15 msec)	None
Transparent — HOR/VERT Blanking	Holding Latches	Slow	Load Update Addr Check Ready Bit	Medium (~50 μsec)	None
Transparent ϕ_1/ϕ_2 Interleave	Very Little	Fast	Load Update Addr	Only for Software	None

Figure 1-3. Comparison Summary

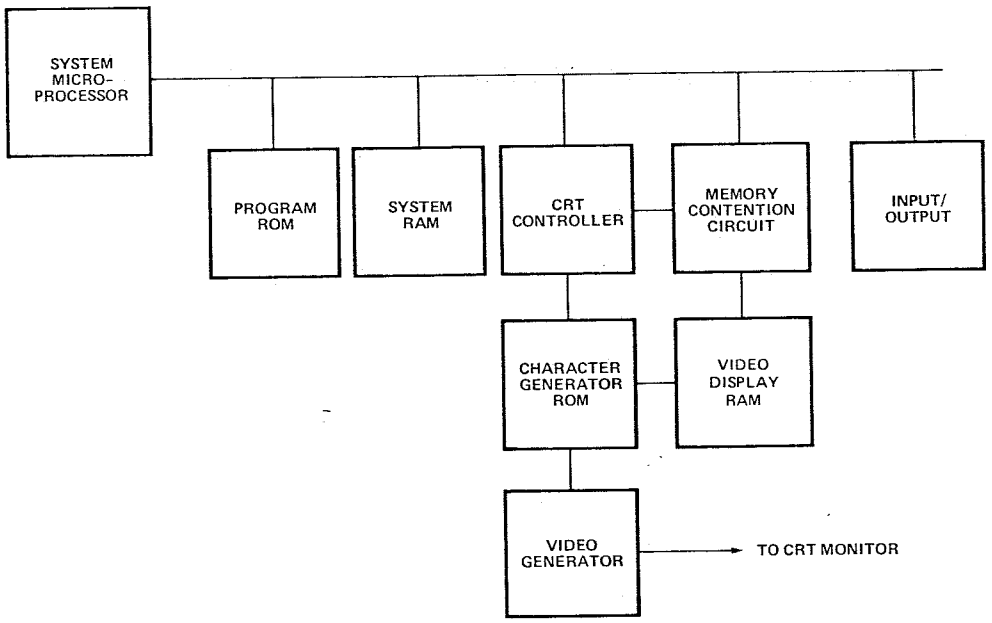

Figure 2-1. Conventional CRT Display System

2.0 Transparent Addressing

One unique characteristic of the SY6545 is its ability to address the screen refresh memory transparent to the microprocessor. The implications of this capability and its impact on system design are described in this section.

2.1 What is Transparent Addressing?

A conventional CRT raster-scan display system is shown in Figure 2.1. Of special interest is the Video Display RAM.

This term is commonly used to designate the memory required to store the displayed screen information, typically ASCII-coded alphanumeric characters. A primary function of the CRT Controller is to constantly retrieve characters from the Video Display RAM and to control the video generation circuits so the display stays active. Thus, the CRT Controller must have access to the Video Display RAM. A difficulty arises, however, since the microprocessor must also have access. Hence, this duality must be resolved and this is achieved by means of the Address Contention circuit.

A variety of address contention circuits may be devised, but they all require additional system hardware in their implementation. A better scheme would be to provide a CRT Controller capable of handling both normal screen refresh and processor accessing of the Video Display RAM. This is accomplished with the SY6545 and is shown in Figure 2-2. This capability is termed Transparent Addressing, because the Refresh RAM now appears to the microprocessor as a port, instead of a block of memory, and, thus the address field is transparent to the microprocessor.

2.2 How Is It Implemented?

A convenient way to begin understanding how the SY6545 handles transparent addressing is to consider the pinouts of the device, as shown in Figure 2-3.

The pin functions can be segregated into five functional groups:

- Power — +5 and ground
- Processor Interface — $\phi 2$, R/W, CS (chip select), RS (register select), and DB0-DB7 (data bus). Permits communication with system processor.
- Video Interface — VSYNC vertical, HSYNC (horizontal), DISPLAY ENABLE, CURSOR, LPEN (light pen strobe), $\overline{\text{RES}}$ (frame synchronization), and CCLK (character clock).
- Character Generator Interface — RA0-RA3 (scan line count). Used as a part of character generator (ROM) address input.
- Video Display RAM control — MA0-MA13 (address), UPSTB (update strobe for transparent address functions).

The pins of primary interest are those in the Video Display RAM control group. The fourteen pins, MA0-MA13, are used to address the Video Display RAM directly (no memory contention circuits needed). This accommodates up to 16K addresses; in other words, up to 16K characters may be contained in the RAM. These addresses normally cycle from some programmable start address to an end address determined by the number of characters displayed on the screen. This scan is continuous, in order to keep the screen display active. Updates to the screen

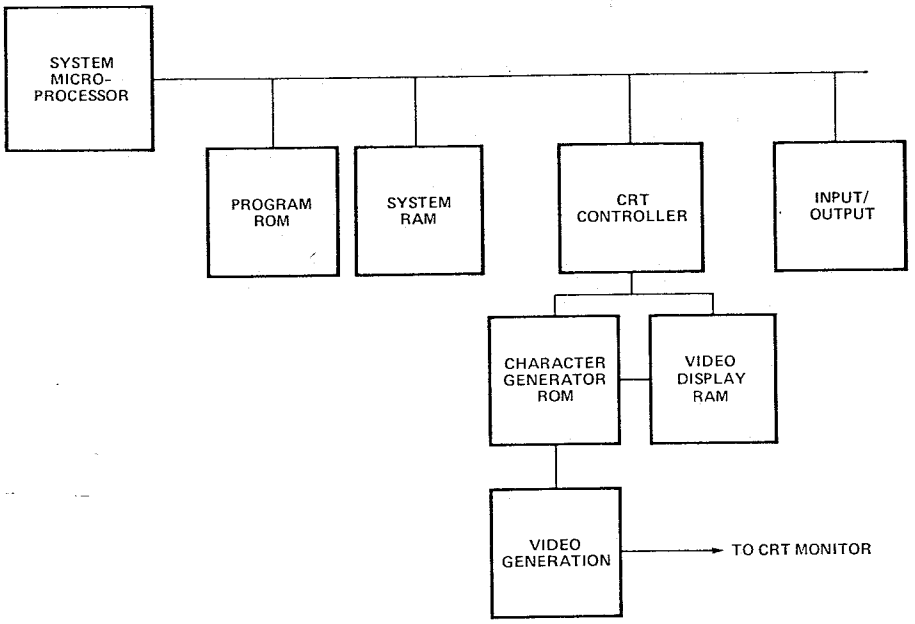

Figure 2-2. CRT Display System with Transparent Addressing

display are accomplished by storing new data in the Video Display RAM. To achieve this, the processor must first send the memory address to be updated to the 6545 and the update data character to an external latch. The 6545 then puts out the update address on the MA lines and a strobe on the UPSTB lines to activate the update. It should be clear, then, that the actual update character does not go through the 6545, but instead, the 6545 only controls the addressing and the gating for the character to be stored in the RAM.

2.3 When Does Character Updating Occur?

Although transparent addressing eliminates the need for memory contention circuits, it is still necessary to define the memory update (and memory read) scheme to use this capability effectively. There are two convenient ways to accomplish updating which have no effect on the visual quality of the display. They are:

- Interleaved ϕ_1/ϕ_2 Updates (Figure 2-4)
  - — In this mode, the ϕ_1 portion of the processor cycle is used for normal screen display functions. The ϕ_2 portion is used for processor updates to the Video Display RAM
- Retrace Updates (Figure 2-5)
  - — In this mode, the horizontal and vertical retrace (blanking) periods are used for processor updates to the Video Display RAM

Each of these techniques has its own advantages and drawbacks. These are outlined in the next sections.

2.4 ϕ_1/ϕ_2 Clock Cycle Interleaving for Updates

The fundamental basis for interleaved RAM accessing is that the 6502 (and 6800) clock cycle consists of two equal portions, ϕ_1 and ϕ_2, and that ϕ_2 is normally used for MPU data bus operations and ϕ_1 is optionally available for special functions.

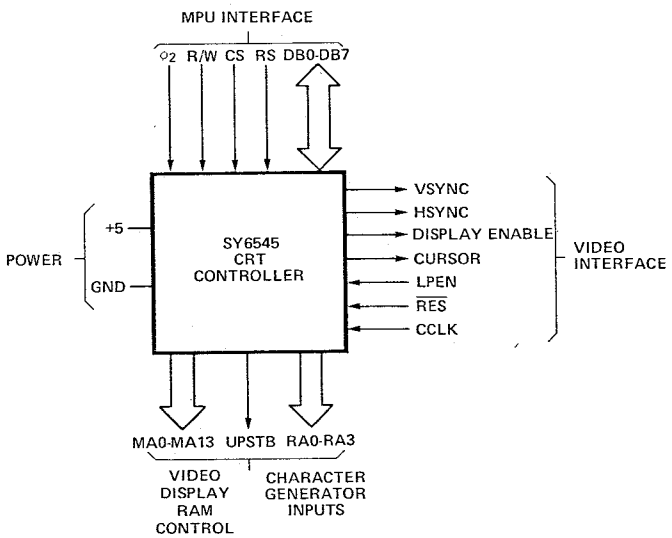

Figure 2-3. SY6545 Pin-Outs

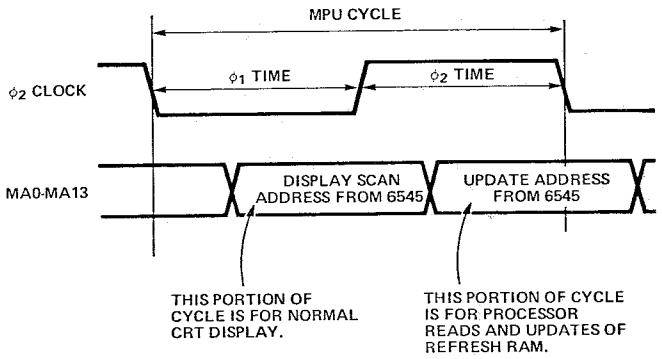

Figure 2-4. Interleaved ϕ_1/ϕ_2 Clock Timing

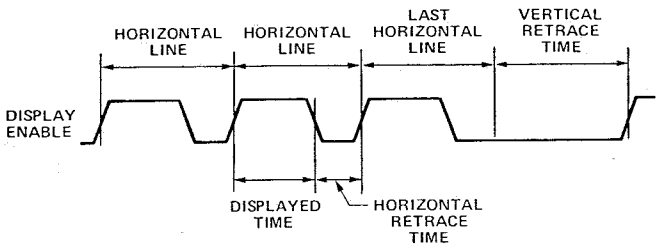

Figure 2-5. Retrace Timing

The ϕ_2 portion of each clock cycle is always made available to the system MPU, while ϕ_1 is dedicated to normal CRT screen refresh functions. Thus each ϕ_1 cycle is used by the CRTC to fetch character data from the Video Display RAM to keep the display active. The ϕ_2 portion is used for all MPU operations, among them being access to the Video Display RAM to perform read and update cycles.

A unique requirement of this mode is that the MPU clock (ϕ_2) must be synchronous with the screen character clock (CCLK). No degree of asynchronism is allowed. This means, then, that the system MPU must not be permitted to free run, but must be slaved to the character clock.

Since the dot rate of the display is fixed by the screen display parameters, this determines the CCLK rate, also. The MPU must not run slower than the CCLK rate, but must be either equal to it or an even multiple faster rate. In most cases, the CCLK rate will be around 1-2 MHz. Under these conditions, equal CCLK and MPU clock rates work quite well.

One additional requirement of the CRTC for this mode is that the Video Display RAM address lines (MA0-MA13) switch between the display scan address (for screen data) and the read/update address (for MPU operations). This is automatically done by the SY6545 when this mode is selected and results in the ϕ_1 portion of the clock cycle with the scan address on the MA lines and the ϕ_2 portion, with the contents of the Update Address Register of the CRTC on the MA lines. Thus, any MPU operation on the Video Display RAM will be done on the programmed update address and will be independent of the display scanning function. Figure 2-6 illustrates the timing for this mode, when the CCLK and MPU clock rates are equal.

Several points are noteworthy, regarding Figure 2-6:

- ϕ_2 causes the multiplexing between the scan address and the update address.
- CCLK advances the scan address on each occurrence of a CCLK pulse.
- Video Display RAM select (either read or write) causes the update address to increment. This simplifies operations which require updating or reading a long sequence of screen characters.
- Because of the propagation delay from ϕ_2 clock edges to the MA lines switching, care must be taken to ensure fast enough RAMs to respond to the relatively short access time requirements which result.

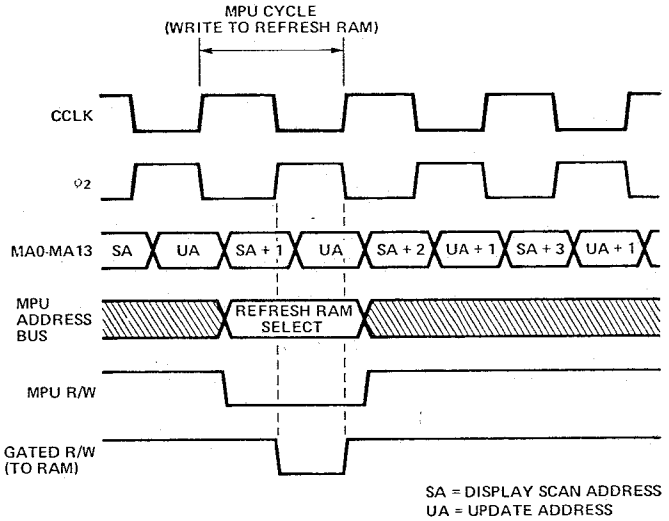

Figure 2-6. ϕ_1/ϕ_2 Clock Interleaving — Update Timing (Note: UA is update address, SA is scan address)

A variation of the scheme has the character clock rate as a multiple of the ϕ_2 clock. In this way, character fetches are not made in every MPU cycle, but at some slower rate. Synchronism must still be maintained, however, between the ϕ_2 clock and the Character Clock. Timings for this mode are shown in Figure 2-7 for the case of the Character Clock rate being 1/2 of the ϕ_2 clock rate. It should be noted that the ϕ_1 portion of the cycle always contains the scan address, even though the scan counter does not advance each cycle.

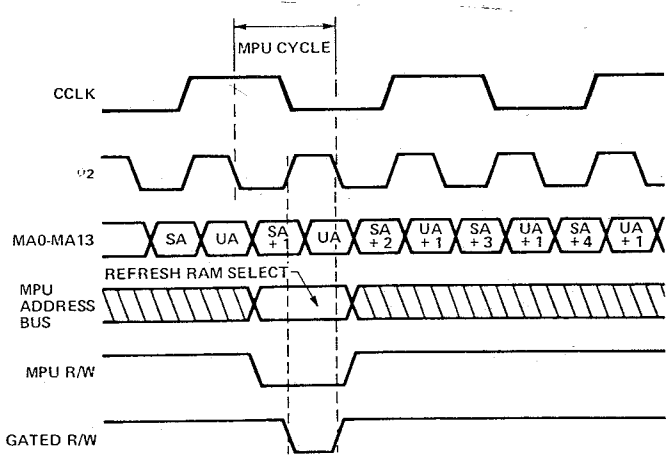

Figure 2.7 Synchronous Interleaving with Unequal Clock Rates

2.5 Special Considerations for ϕ_1/ϕ_2 Interleaved Mode

Reading and writing (updating) of the Video Display RAM requires some system considerations which are not immediately obvious. Since the update address in the 6545 is always present on the Video Display RAM address lines during the ϕ_2 portion of the cycle, the MPU can perform read/update operations directly on the RAM by selecting it as if it was an I/O port. The RAM select must be an address in the MPU address field, but individual character location addresses are generated by the 6545. This is the simple part of the operation. Problems arise when it is desired to update (or read out) a large number of sequential RAM locations. The update address register in the 6545 functions as an incrementing counter, but will only increment if the 6545 "knows" that a read/update has occurred. The facility for this has been provided in the 6545 by means of the "dummy" data register. When the "dummy" register is selected as the destination of data, then when a 6545 select occurs, this is interpreted by the 6545 as a RAM read or update and the update counter is incremented. As long as this register is the destination address programmed in the 6545, then subsequent 6545 selects will continue to increment the counter. Thus, the RAM and 6545 selects must be related in a very specific fashion:

- The RAM select must also cause a CRTC select, so that the CRTC update counter can be advanced.
- The CRTC select must not cause a RAM select, in order to permit CRTC operations to occur without affecting the RAM.

An address scheme which exemplifies how this requirement can be achieved is indicated in Figure 2-8.

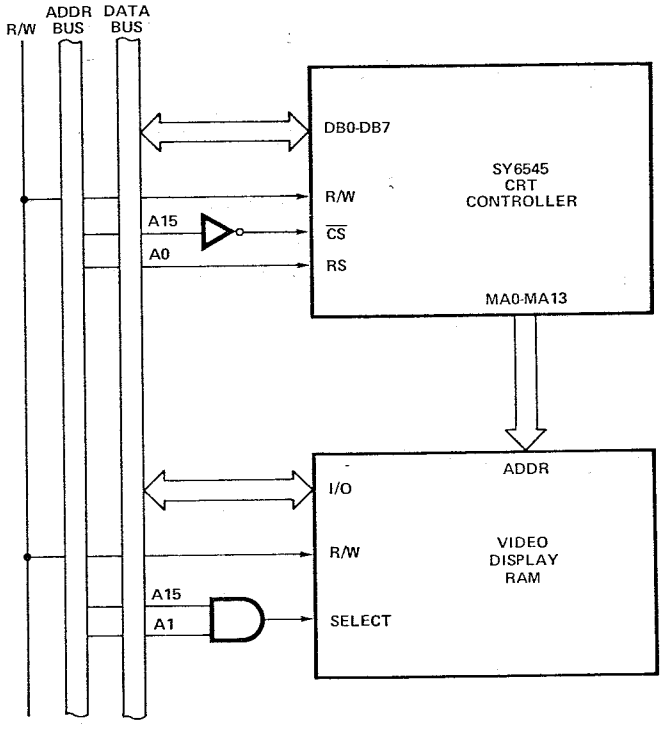

Figure 2.8 Addressing Relationship for 6545 and Video Display RAM

In the example of Figure 2-8, it can be seen that the following addressing occurs.

HEX ADDR	A15	A1	A0	CRTC Selection	RAM Selection
8000	1	0	0	Address Register	Unselected
8001	1	0	1	Register Programming	Unselected
8003	1	1	1	Increment Update Counter (if dummy register selected)	Selected

In this way, the address requirements outlined previously have been achieved. Other schemes can be used, as well, since this is only a single example to demonstrate a typical solution.

It should be recognized that Interleaved Updates optimizes processor performance by always permitting immediate RAM updates or reads to occur. However, there is a penalty; the RAM devices used must be fast enough to respond to the split-cycle accessing. Furthermore, the processor cycle time must be carefully selected and is not independent of the screen character rate, but an exact multiple of it.

2.6 Retrace/Blanking Intervals for RAM Read/Updates

An alternative to using Interleaving to perform refresh RAM updates is to use the horizontal and vertical retrace periods. This is selected in the 6545 as a programmable operating mode.

Using the retrace intervals for read/updates simplifies the timing and control circuits required but may impact MPU efficiency slightly, since updates do not occur immediately and require some additional program steps to check status bits.

Another requirement is the use of the Update Strobe from the CRTC to synchronize read/updates with the update address on the RAM address lines.

The timings in Figure 2-9 indicate the relationship of the Update Strobe, the Update Address, the Display-Enable, and the Character Clock. The update address is gated on the RAM address lines immediately after the display is blanked and stays for three character clock cycles. The Update Strobe is one character clock in duration and is centered within the update address. Its function is to signal the Data Bus Latch/Buffers to perform the required read/update operation.

The same chip-select considerations apply for this mode as for the ϕ_1/ϕ_2 Interleave mode. Likewise, the dummy register also is utilized to inform the 6545 when RAM select conditions occur.

Several noteworthy points should be understood before advancing to more detail on this update scheme.

- The Display Enable signal is high during CRT display times and low during horizontal or vertical blanking periods. Typically, the low portion of this signal might be about 20μsec (horizontal blank) and the high portion, about 40 μsec for each line. The vertical blank might be about 5 msec every frame time (17 msec/frame).

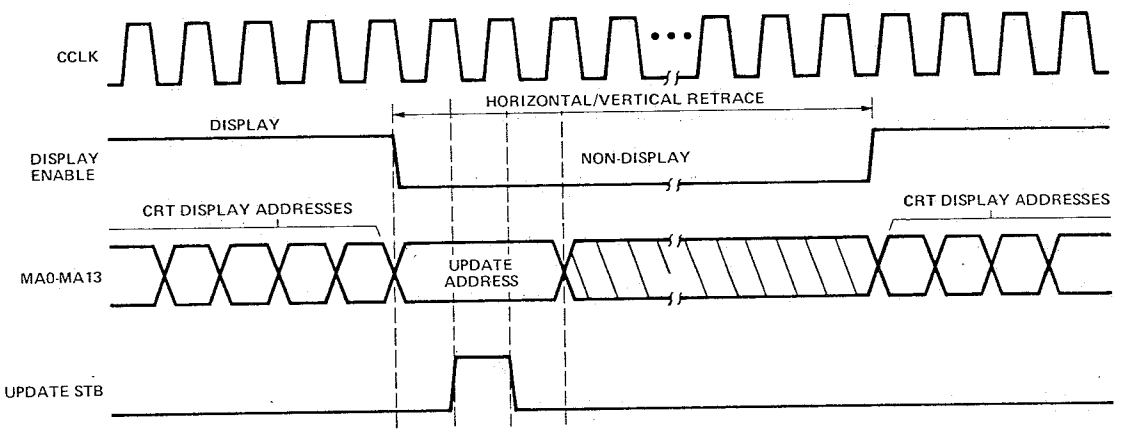

Figure 2-9. Retrace Update Timings

- The Ready bit in the Status Register goes low (not-ready) whenever the dummy register is first selected and whenever the RAM Latches are selected with the read or write commands. The Ready bit goes high whenever an automatic read (AR) of the RAM occurs.
- The RAM Latches are used for:
  a. To store the 8 data bits to be written when an MPU-write occurs.
  b. To store the 8 bits on an automatic read (AR) in anticipation of an MPU-read operation.
- The Update Address Counter (UAC) in the 6545 is incremented whenever an Update Strobe occurs in response to a RAM write and whenever a RAM read occurs.

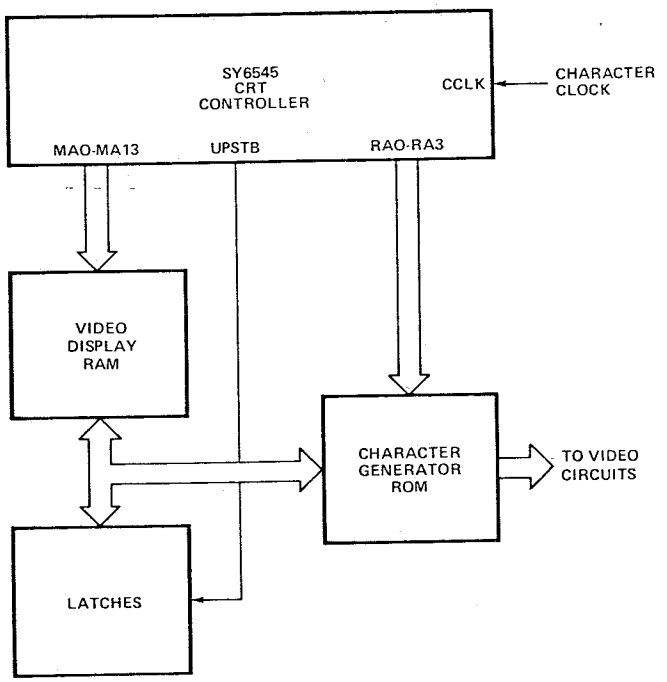

Figure 2-10. Simplified Diagram for Retrace Updates

Figure 2-10 illustrates the use of the UPSTB signal to control the data-bus latches.

The relationship of the CCLK, Display Enable, MA lines, UPSTB, and Ready bit in the 6545 status register is shown in Figure 2-11, an example of timings for successive read operations. The key items to note are:

- The use of the UPSTB to key all hardware operations
- The use of the Ready bit to key all software operations

The function of the Ready bit must be clearly understood:

"1" (READY)
Signifies that the RAM latches contain the data stored in the RAM address of the UAC. Thus, the RAM latches may be read by the MPU or they may be written if it is desired to store new data in the RAM. In the latter case, the data is not stored immediately, but is retained until the next available retrace time.

"0" (NOT-READY)
Signifies that the 6545 is either waiting to store data into the RAM or is waiting for the next automatic read from the RAM. In either case. The MPU may not write into or read from the RAM latches during the "not-ready" time.

Figure 2-12 shows another timing example; this one for the case of successive RAM write operations (updates).

Of particular interest is that memory writes always cause a double update cycle to occur, whereas reads cause only single updates. This is apparent in Figure 2-12 and is required because the 6545 must anticipate the processor will do a read operation and must pre-load the latches with the RAM data so that, if the processor does, indeed, read the data, it is already there and no processor delay is encountered. If, however, the processor does a write operation, this is no problem, since the data in the latches is ignored and is, in fact, lost.

For example, in Figures 2-11 and 2-12, the scan is assumed to be in the non-display (retrace) time, entirely. In a real situation, updates may be desired which take more time than is available during a retrace period. This conflict is resolved by the Ready bit in the 6545, which

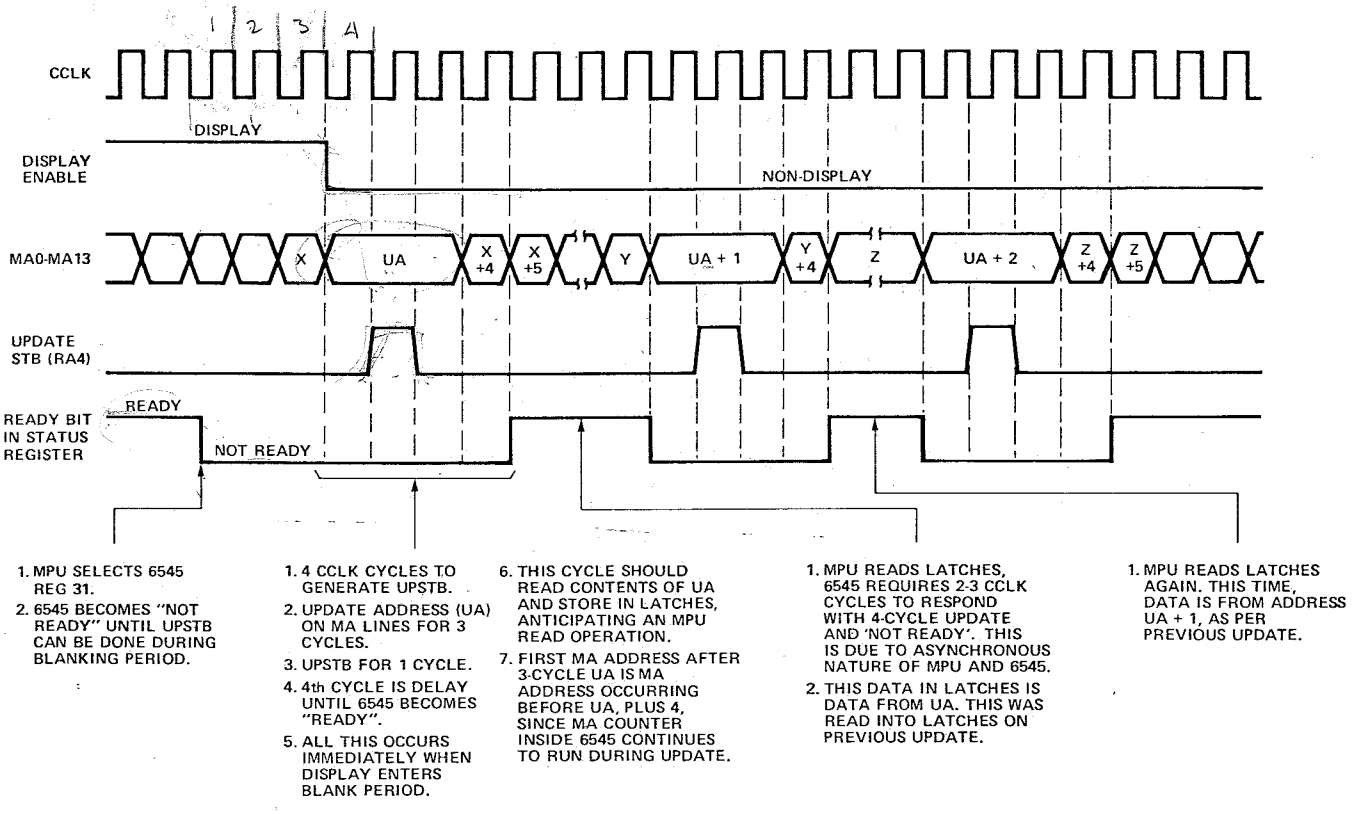

Figure 2-11. Timing for Successive Memory Reads as Scan Starts Non-Display Period

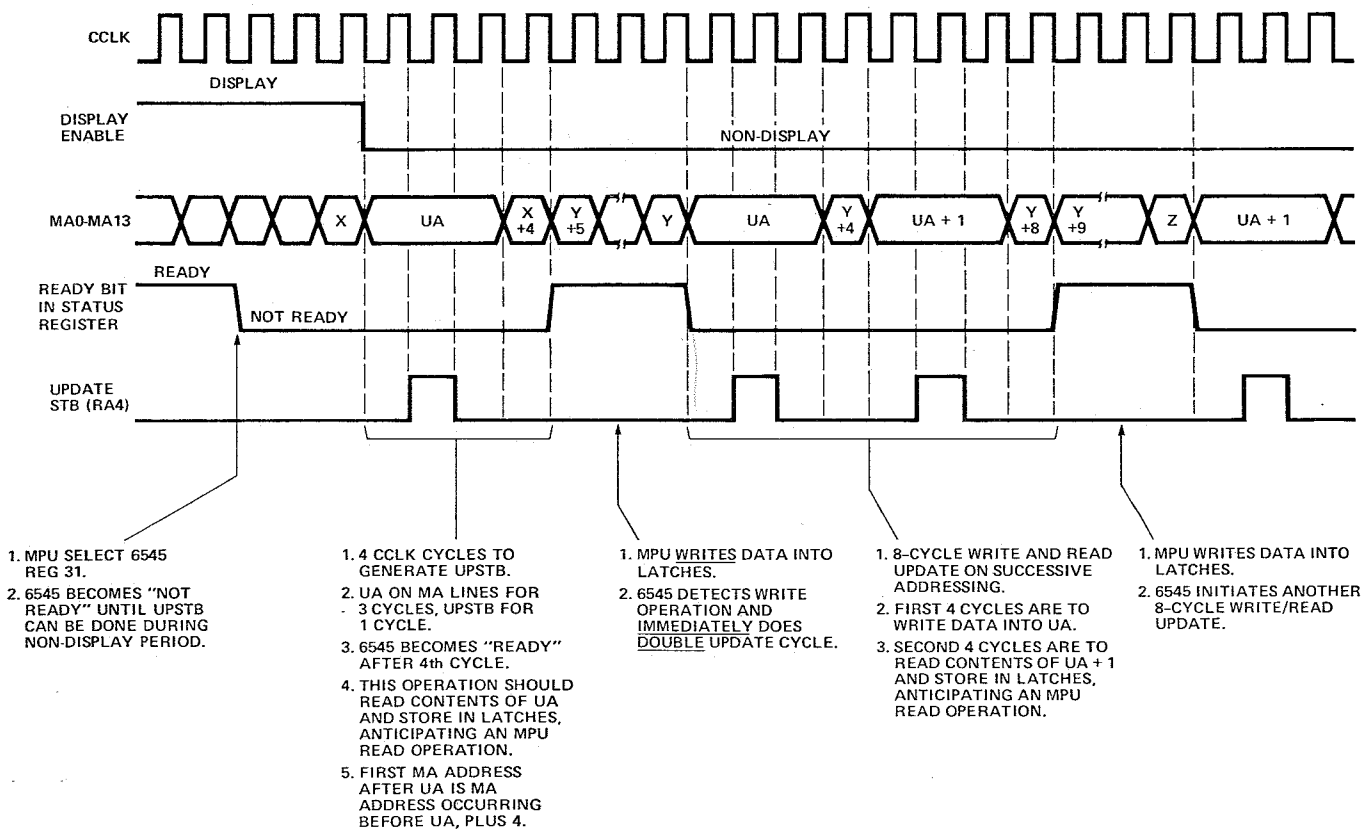

Figure 2-12. Timing for Successive Memory Writes as Scan Starts Non-Display Period

simply stays "not ready" until the next available retrace time, so no special processor considerations must be made.

Figures 2-13 through 2-15 illustrate the timings which result when update cycles occur very near the end of a non-displayed time interval. In Figures 2-13 and 2-14, the update is performed before the display becomes active (although in Figure 2-14, the cycle is truncated) and in Figure 2-15, the update is aborted and delayed until the next occurring non-display time.

2.7 Summary

Transparent addressing has been presented as a technique to simplify CRT system designs and has been shown to be a unique feature of the Synertek SY6545 CRT Controller device. Two schemes were presented to implement Refresh RAM updating and reading:

- Interleaving optimizes system software at the expense of more complex timing and fast memory.
- Using Blanking/Retrace times for memory access simplifies hardware requirements, but needs more software and may not be fast enough for certain CRT applications.

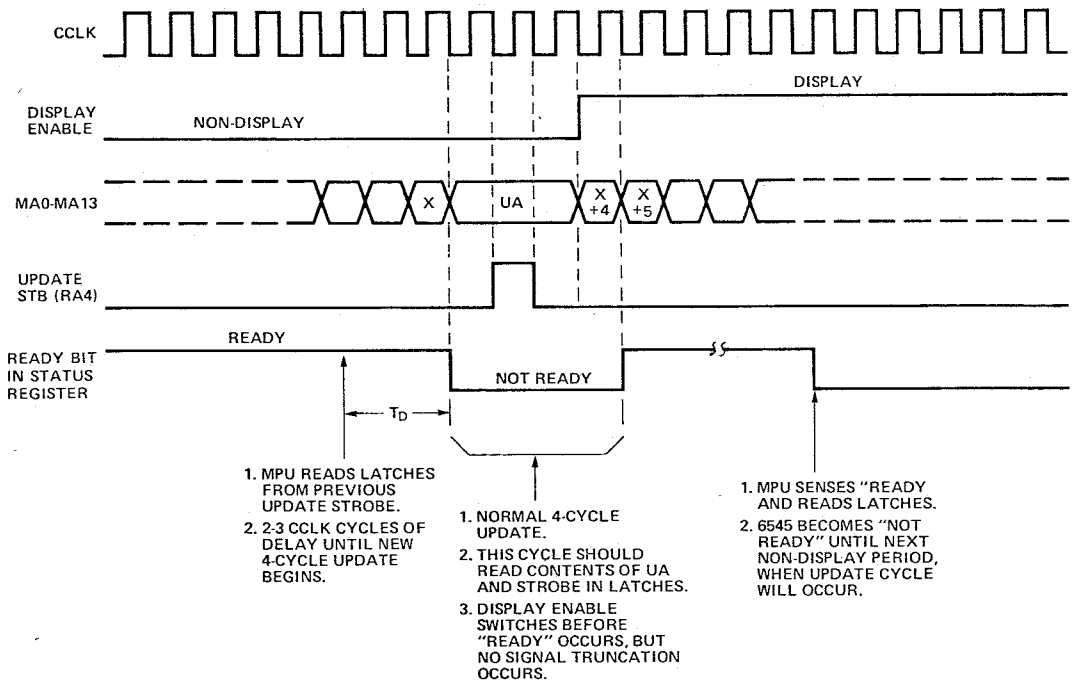

Figure 2-13. Memory Read at End of Non-Display Period (No Truncation)

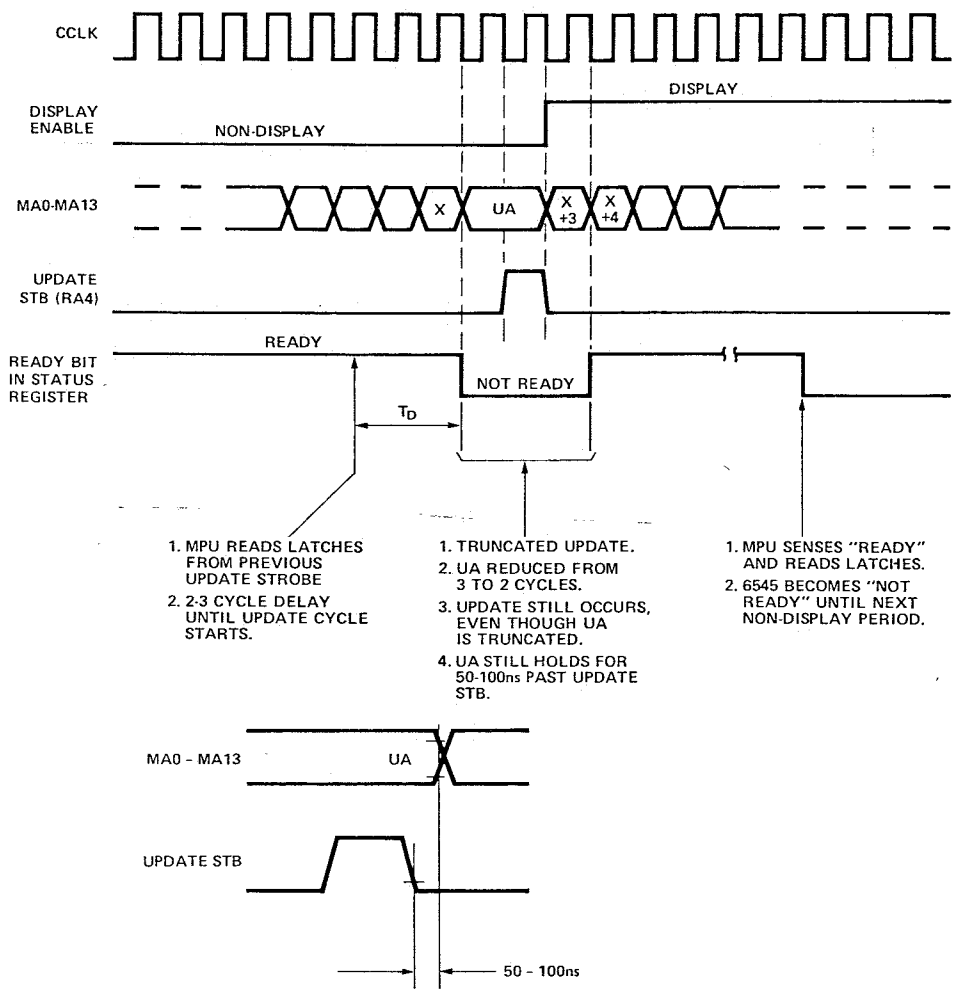

Figure 2-14. Truncated Memory Read at End of Non-Display Period

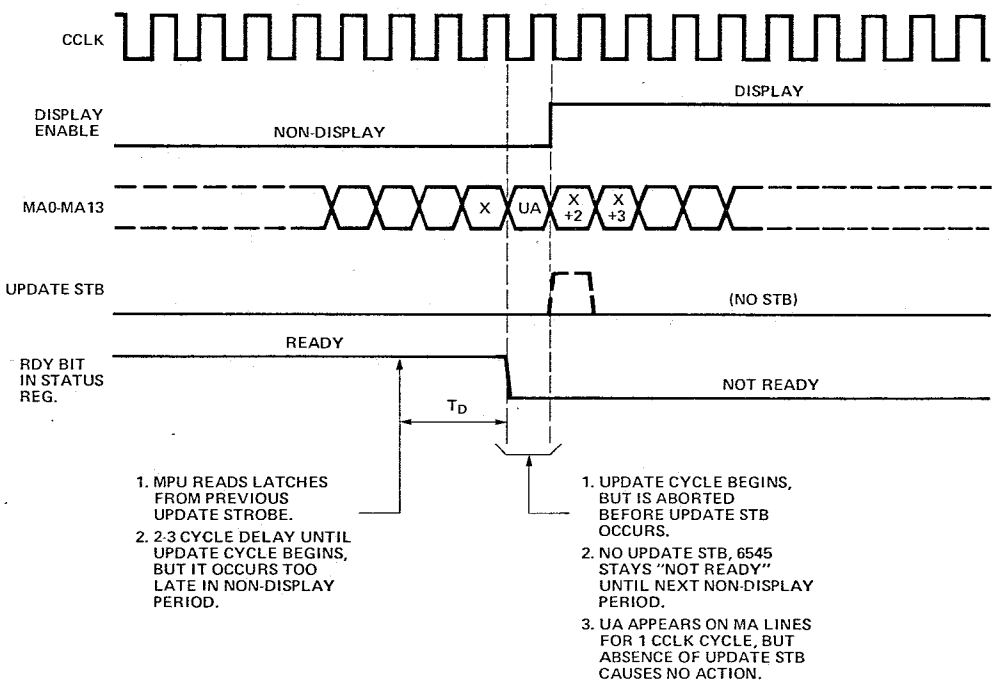

Figure 2-15. Aborted Memory Read at End of Non-Display Period

3.0 Frame Synchronism Using $\overline{RES}$

The frame frequency of a CRT display is the rate at which the entire screen is scanned. It is necessary for this rate to be equal or nearly equal to the line frequency (50 or 60 Hz) in order to minimize video flicker effects.

3.1 Without using $\overline{RES}$

It is possible to achieve very close line frequency synchronism without using the $\overline{RES}$ signal on the SY6545. This is accomplished by carefully selecting the character clock (CCLK) rate and by programming the display format registers in such a way that the total time for the display counting sequence is very nearly equal to 1/f (16.7 msec for 60 Hz and 20 msec for 50 Hz). If the resulting frame rate is within 2-3% of the line frequency, then the display will have reasonably good appearance.

3.2 Using $\overline{RES}$ For Exact Synchronism

The function of the $\overline{RES}$ input signal is to force all internal counters to their initial state, regardless of where they currently are in their counting sequence, and to start the scan when the signal is released. Thus, if the frequency of $\overline{RES}$ is locked by the line frequency, the display may be synchronized exactly. This can be achieved by using a zero-crossing detector circuit to respond to line frequency cycles and to generate a single pulse each cycle. Figure 3-1 illustrates the waveforms.

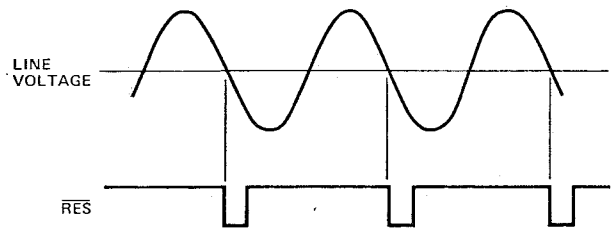

Figure 3-1. $\overline{RES}$ Generated from Line Voltage

3.3 Register Programming if $\overline{RES}$ is Used

If $\overline{RES}$ is utilized for frame synchronism, then it is necessary to program the SY6545 formatting registers slightly differently. The main objective will be for the display scanning counters to count for a period slightly longer than the $\overline{RES}$ rate. In this way, when a $\overline{RES}$ signal occurs, the counters should still be running and should not have reached the end of their sequence. $\overline{RES}$, then, will restart the counters, and synchronism will be achieved. A facility is available for this in the SY6545 by virtue of REG 5, which permits a selectable number of extra non-displayed scan lines to be added to the sequence.

3.4 Synchronizing $\overline{RES}$ With CCLK

The nature of $\overline{RES}$ requires careful synchronism with CCLK in order to assure proper system operation. The effect of $\overline{RES}$ is specifically outlined as follows:

- The high-to-low transition of $\overline{RES}$ causes the MA0-MA13 and RA0-RA4 outputs to immediately stop counting and to go to a low level
- The low-to-high transition of $\overline{RES}$ causes the MA0-MA13 and RA0-RA4 outputs to immediately take the state of the Starting Address register-pair in the SY6545 (R12 and R13). Further, this transition immediately enables the CCLK to the internal counters, so the next occurring high-to-low CCLK edge increments the counters.

The effect of the $\overline{RES}$ low-to-high transition, if asynchronous relative to CCLK, is that the first address after $\overline{RES}$ will have an undetermined duration, depending on where in cycle the transition occurs. Figure 3-2 illustrates this.

A better way to operate $\overline{RES}$ is to synchronize it with CCLK. If $\overline{RES}$ transitions are clocked so that the actual $\overline{RES}$ to the SY6545 occurs at the next occurring CCLK high-to-low edge, then no address cycle truncation will result. Figure 3-3 illustrates this.

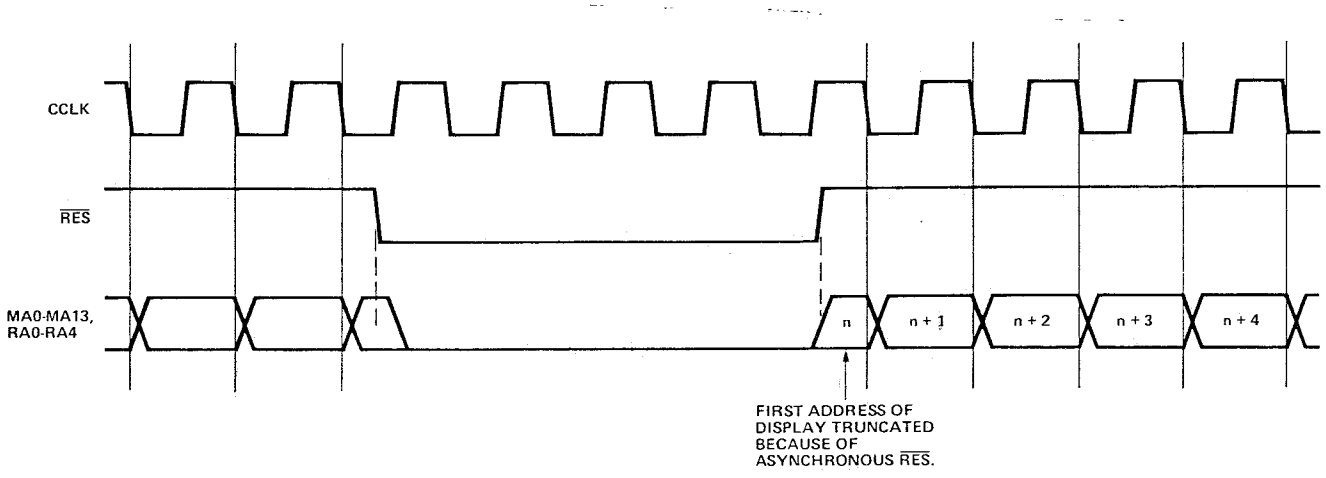

Figure 3-2. Timings with Asynchronous $\overline{RES}$ and CCLK

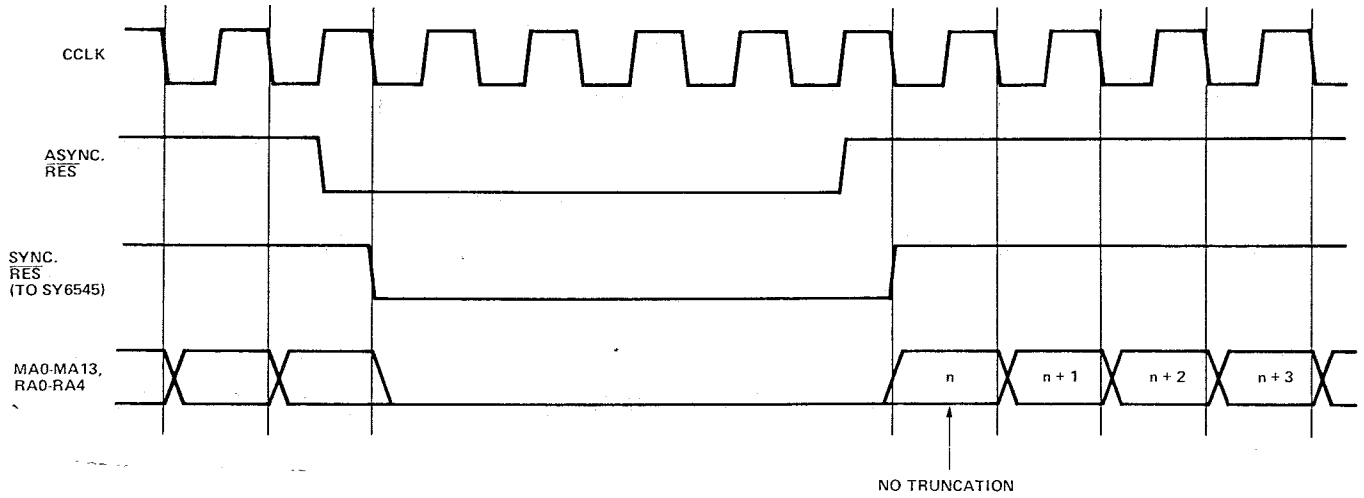

Figure 3-3. Timings with Synchronism Between $\overline{RES}$ and CCLK

4.0 Split-Screen Displays

The SY6545 CRT Controller fulfills most requirements for raster-scan display system designs. Certain display applications, however, present special problems requiring novel solutions.

One such application is split-screen displays. The basic concept of a split-screen display is illustrated in Figure 4-1.

The diagram on the left illustrates a conventional display, characterized by a text area composed of rows and columns of alphanumeric characters. The split-screen display, however, consists of both a left and a right side text area. The real complication of implementation of a split-screen CRT control system arises when special requirements of such a display are tabulated:

- Left and right side texts must have independent scrolling
- Left and right side text memory must be separate and independent

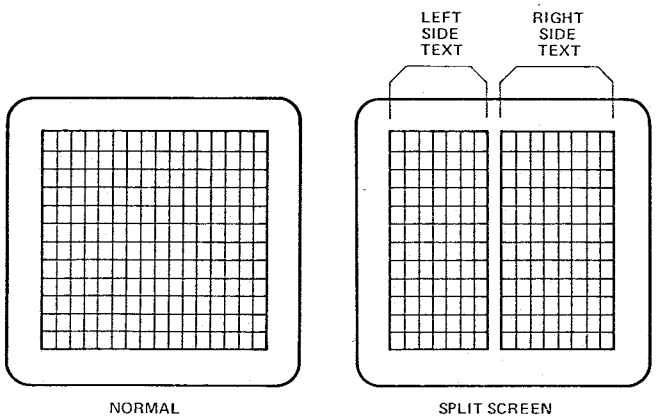

Figure 4-1. Normal vs. Split-Screen Display Illustration

The impact of these requirements is that conventional CRT Controllers, like the SY6545, do not have facilities to accommodate these needs. Special techniques may be employed with the SY6545, however, to achieve split-screen display.

4.1 Functional Requirements

The specific application presented here is assumed to have certain constraints:

- Left and right side texts are comprised of characters of the same size
- The number of columns in each text is variable and they need not be equal
- The space between texts is selectable
- The top row of each text is at the same position
- The number of displayed rows in each text may be different

These constraints are not very limiting and, in fact, permit a great deal of display flexibility. Figure 4-2 illustrates the CRT display timing in simplified form.

For a complete understanding of the display timing, the reader is referred to the SY6545 data sheet. Of special interest, regarding Figure 4-2 is the lower set of waveforms. Note especially, the timing of Display Enable. For each scan line, Display Enable, is true for two separate time intervals: once, for the left side display, and once for the right side. Memory addresses (MA lines) will be non-contiguous for each displayed time; that is the addresses for the left side will not be related to those of the right.

4.2 Logical Implementation

Figure 4-3 shows a simplified logic diagram to implement the split-screen timing of Figure 4-2.

Of special interest in Figure 4-3 is the use of two SY6545 devices to achieve split-screen display control. SY6545 #1 is used for the left side display and SY6545 #2, for the right.

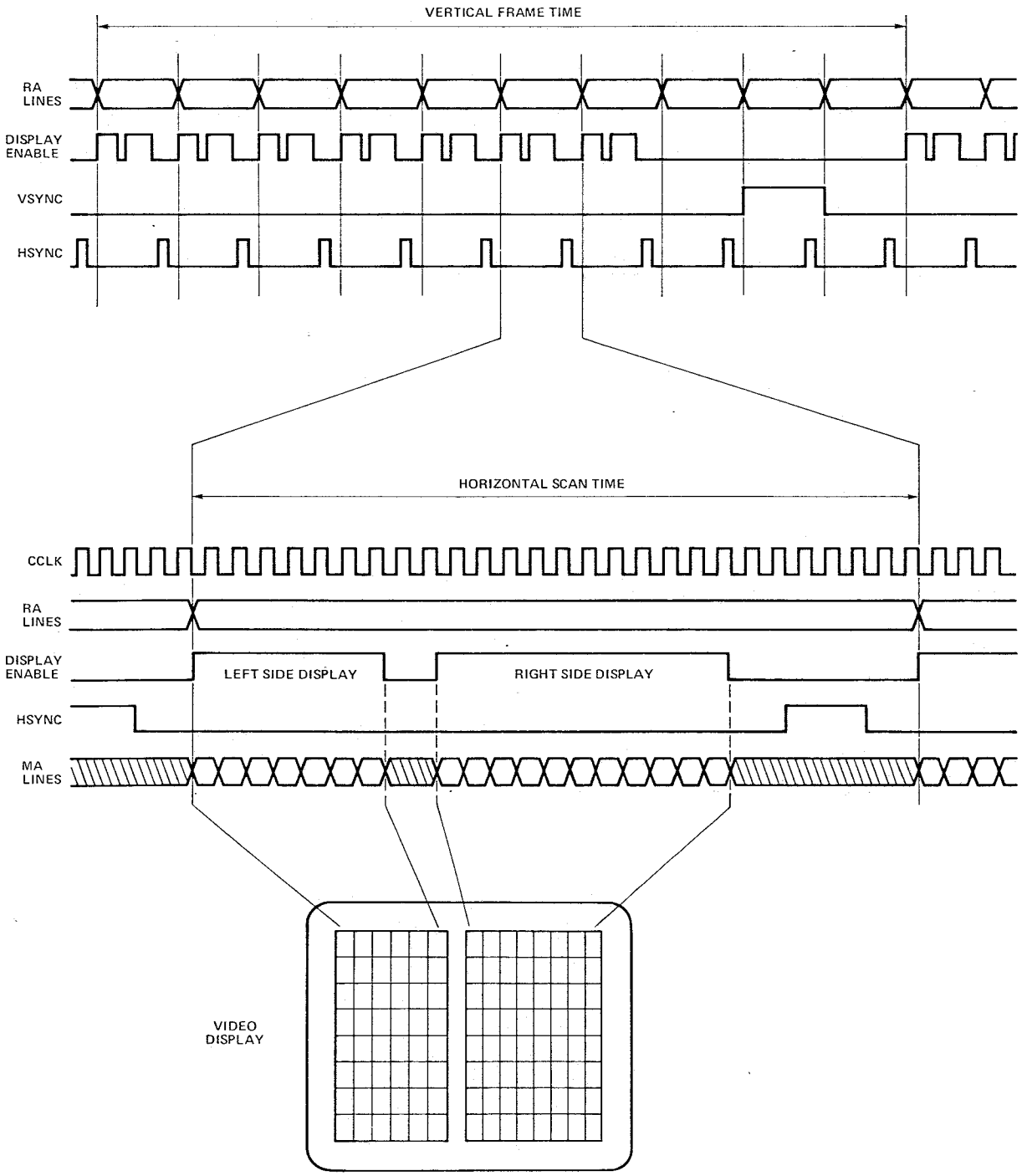

Figure 4-2. Simplified Split-Screen Timing

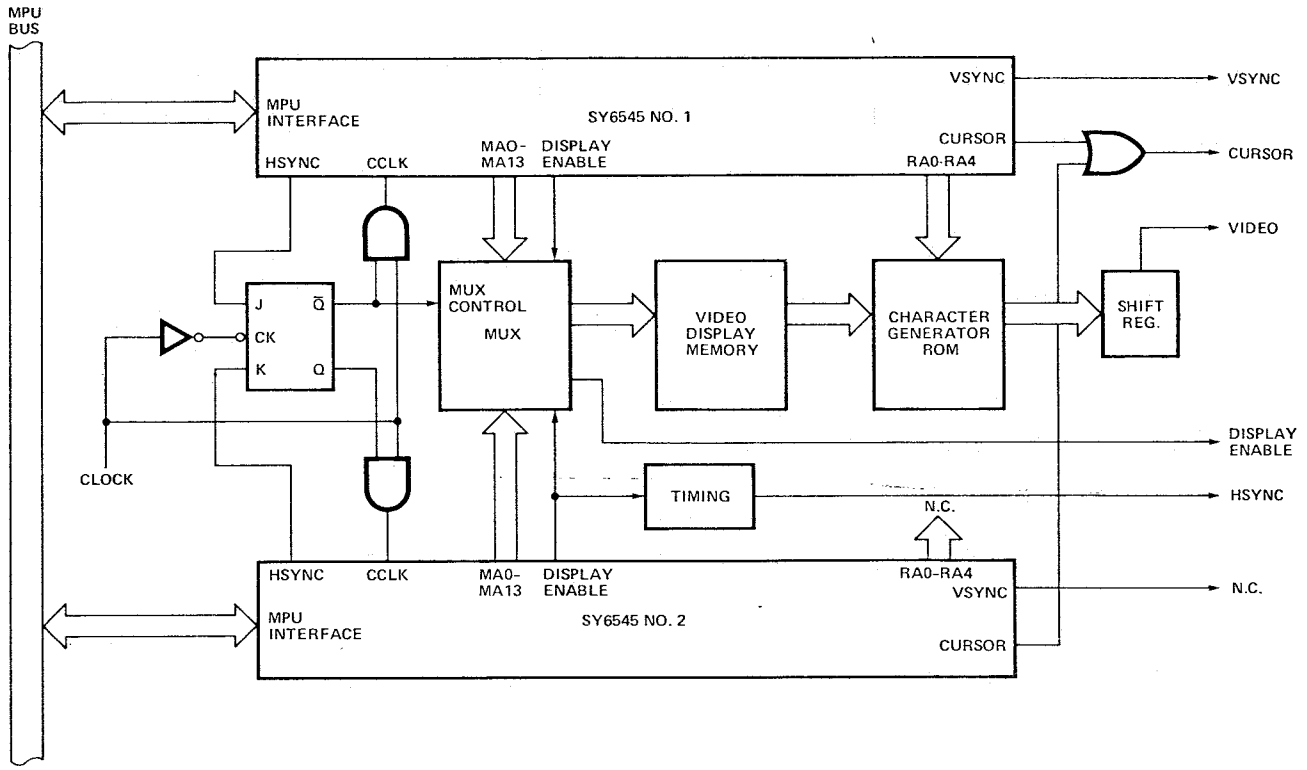

Figure 4-3. Logic Implementation

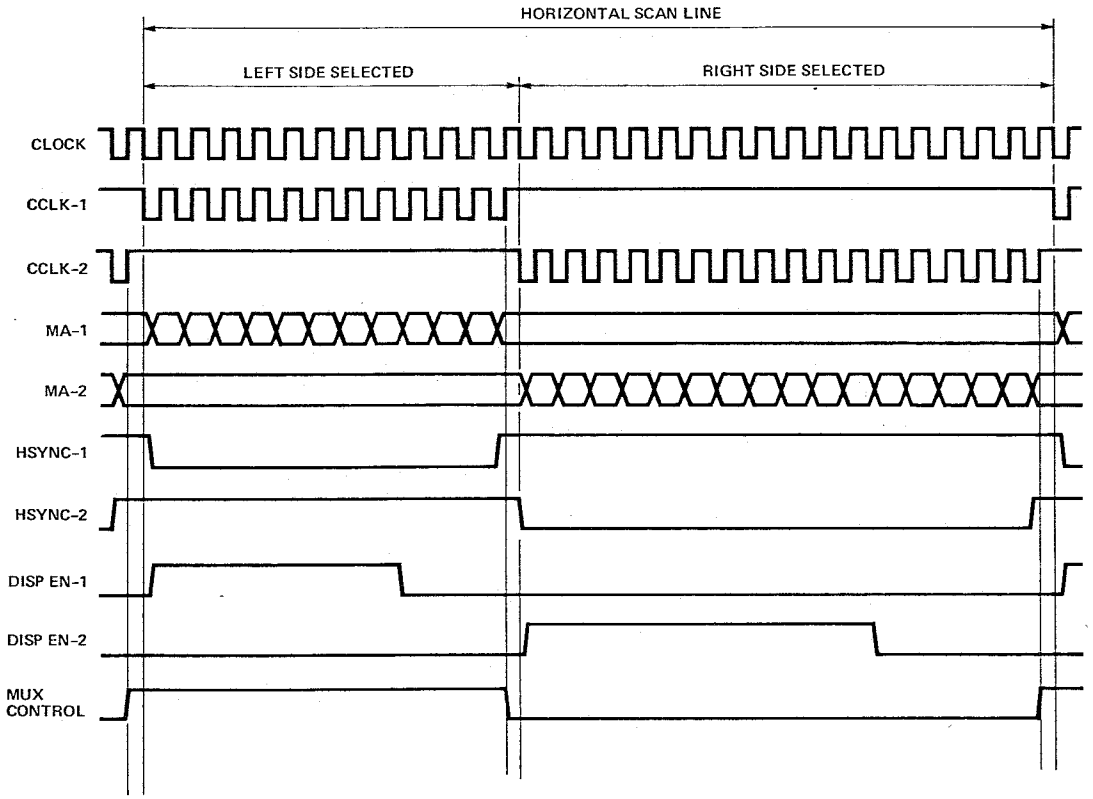

Figure 4-4. Dual-6545 Timing for Split-Screen Display

In this way, addressing sequences are totally separate. Memory allocation and scrolling is thus totally independent.

Switching between addresses generated from each SY6545 is accomplished by the use of the MUX in Figure 4-3. This block must be capable of connecting either set of MA address lines to the Video Display Memory. Figure 4-4 illustrates the timing.

The MUX Control signal, used to switch between the two SY6545 address groups, is generated by the J-K flip-flop, off of the two HSYNC outputs. Further, the MUX Control also permits the CCLK for the selected SY6545 to run. When unselected, the SY6545 CCLK is turned off. The effect of this is that each SY6545 is alternately selected within each raster scan line. In this way, each displayed text is independent of the other.

Some special points are noteworthy:

- The use of the HSYNC signals to control the selection of left and right addresses means that the HSYNC for the display monitor must be generated separately. Figure 4-3 shows this as the Timing block, generated off of the Display Enable signal from SY6545 #2.
- Separate Cursor signals for both left and right displays is achieved directly.
- The RA lines (raster line address) and VSYNC for SY6545 #2 are not needed in the system.
- MPU access to the Video Display Memory has not been accounted for in Figure 4-3, since it is a separate issue, controlled by other factors not relevant to split-screen implementation

4.3 Summary

The scheme presented here may be used to accommodate general left-right split-screen displays. Details have been necessarily omitted in the interest of focusing on the fundamental concepts and techniques.

5.0 Operating at Very Fast Character Clock Rates

In some CRT system applications, it may be necessary to operate at character clock (CCLK) rates in excess of the maximum rate specified for the SY6545 CRT Controller. This section outlines a technique whereby the SY6545 is operated at a speed of one-half the system rate. Thus, the effective character clock rate can be doubled.

5.1 Basic Concept

The method used to achieve this is quite simple. It consists of a configuration wherein the SY6545 accesses two characters in each cycle. The system timing must be arranged to select the two accessed characters one-at-a-time to be displayed. Figure 5-1 illustrates the system architecture necessary for this scheme.

5.2 Hardware Details

The video display memory must be organized in two separate blocks containing alternate, odd and even, character locations. In the example of Figure 5-1, several assumptions are made:

1. The size of the video display memory is 2k bytes. This is enough for a single page of 80x24 display (1920 locations), but is not limited to this size.
2. The memory contention scheme shown permits the MPU to have overriding priority in selecting the video display memory. Other schemes may be implemented as well, but this one is the simplest and allows attention to be focused on the more significant aspects of this method.
3. The video display memory is 8-bits wide. Normal ASCII coding only requires 7 bits, but 8-bits is used in this example.
4. Four raster code lines (RA0-RA3) are shown, indicating that more than 8 scan lines per character row (including row spacing) are used. This is also a system function and is not a limitation imposed on this scheme.
5. 8 horizontal bits per character (including spacing) are also assumed in the example.

A key point to note is the video display memory addressing arrangement. The SY6545 address lines, MA0-MA9, are routed through the address selector block to the memory addresses, A0-A9, of both even and odd memory blocks. In this way, as the SY6545 sequences through its count states, the two memories are accessed simultaneously. The MPU addresses, A1-A10, on the other hand, are routed to these same memory addresses, A0-A9. MPU address, A0, is used to select either the even memory (A0=0) or the odd (A0=1), but not both.

In this way, then, the video display memory is configured as a dual-port memory but, more significantly, each port sees the memory with a different organization. The SY6545 accesses the memory as a 1kx16 and the MPU, as a 2kx8.

5.3 Memory Control Logic

The video display memory control signals must function in the following fashion:

1. The chip selects, $\overline{CS}$, must always both be low (select) when the MPU is not addressing the memory. In this way, the SY6545 will be accessing both memory blocks.
2. When the MPU selects the memory, A11-A15 will correspond to the desired memory map decode combination. A0 will select either the even or the odd block. Thus, one $\overline{CS}$ will be low and the other high (de-select).
3. When A11-A15 correspond to the memory map decode, the address selector must also be switched to drive the memory addresses from the MPU address lines, instead of the SY6545 MA lines.
4. Finally, the video display memory R/W line must be driven by the MPU R/W line, but only when the correct A11-A15 is present.

Figure 5-2 shows the memory control logic for the example of the video display memory block to be selected with A15 low and A11 through A14 high.

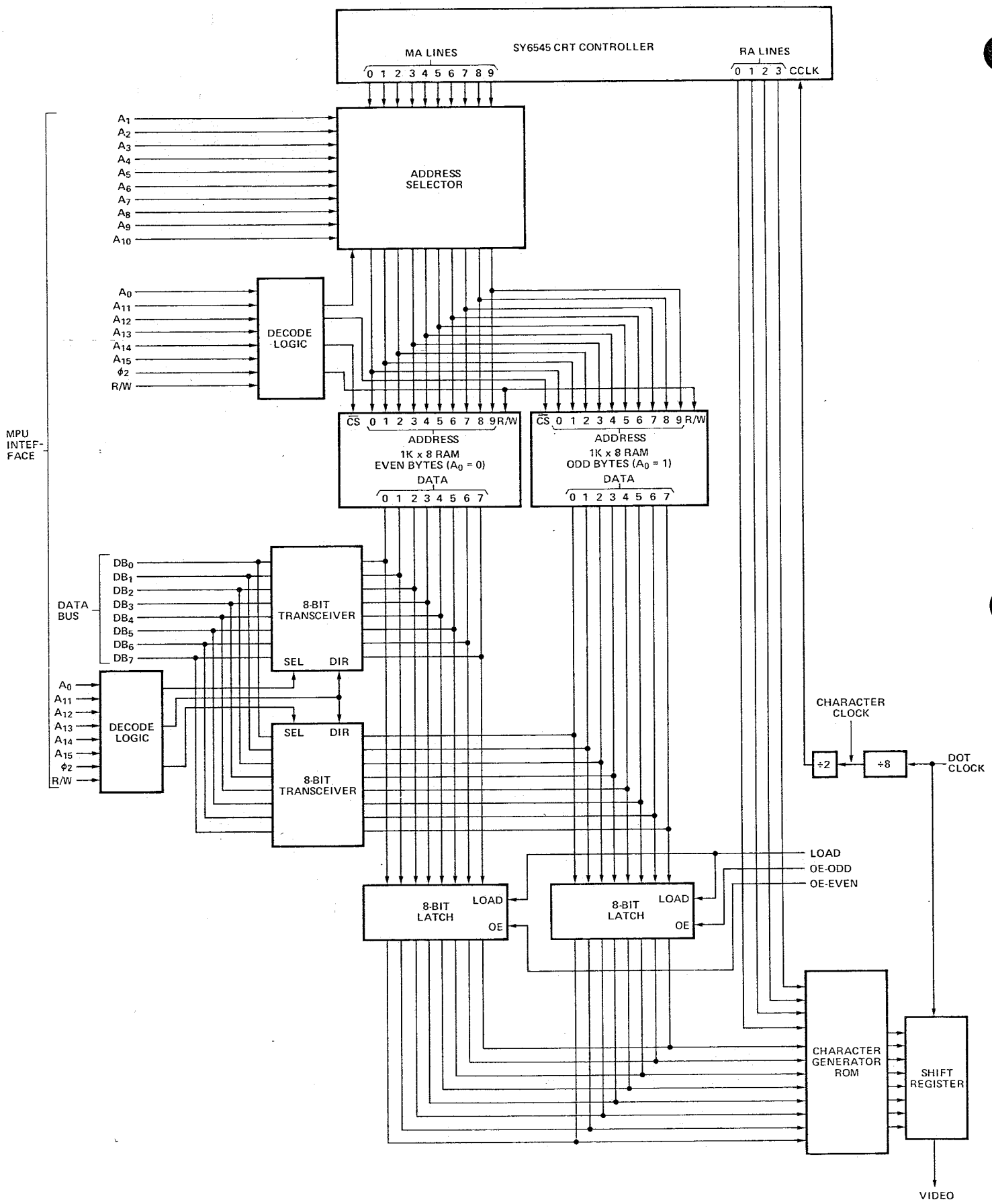

Figure 5-1. System Block Diagram

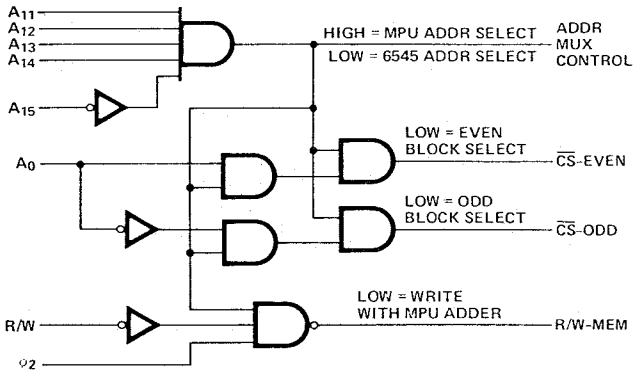

Figure 5-2. Video Display Memory Control Logic

5.4 Data Bus Transceiver Control Logic

The control logic for the odd and even data bus transceivers has similar characteristics to that required for the video display memory.

1. The transceiver selects must also be energized when A11-A15 correspond to the memory map decode. Furthermore, A0 determines whether the odd or even memory block is selected.
2. When A11-A15 do not match the decode pattern, then the transceivers must be unselected and the MPU data bus must be isolated from the video display memory.
3. The MPU R/W line state determines the direction of the data through the transceivers.

Figure 5-3 illustrates the necessary logic for the example presented in Figure 5-2.

5.5 System Timing

Figure 5-4 shows illustrative system timing which further clarifies the detailed operation of this method. The dot clock is the timing signal which is used to drive the shift register for actual video generation. For this example, eight horizontal bits are required for each character. Thus, the dot clock must be divided down to derive the character clock signal. In a conventional system arrangement, this would then be used to drive the SY6545 CCLK pin. However, since this configuration calls for the SY6545 to fetch two characters at a time, the character clock must be halved to derive the CCLK input in the SY6545. In this way, two character clocks generate one CCLK which, in turn, causes two consecutive characters to be fetched, simultaneously, from the video display memory.

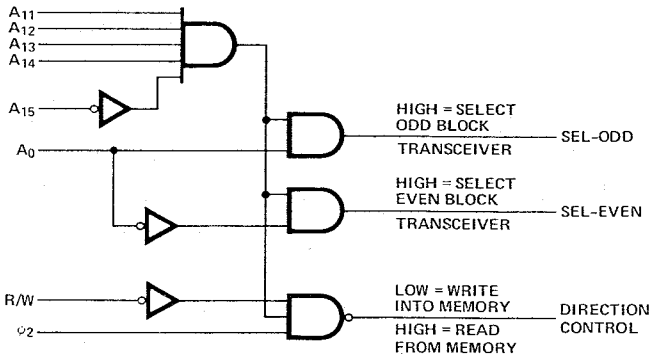

Figure 5-3. Data Bus Transceiver Control Logic

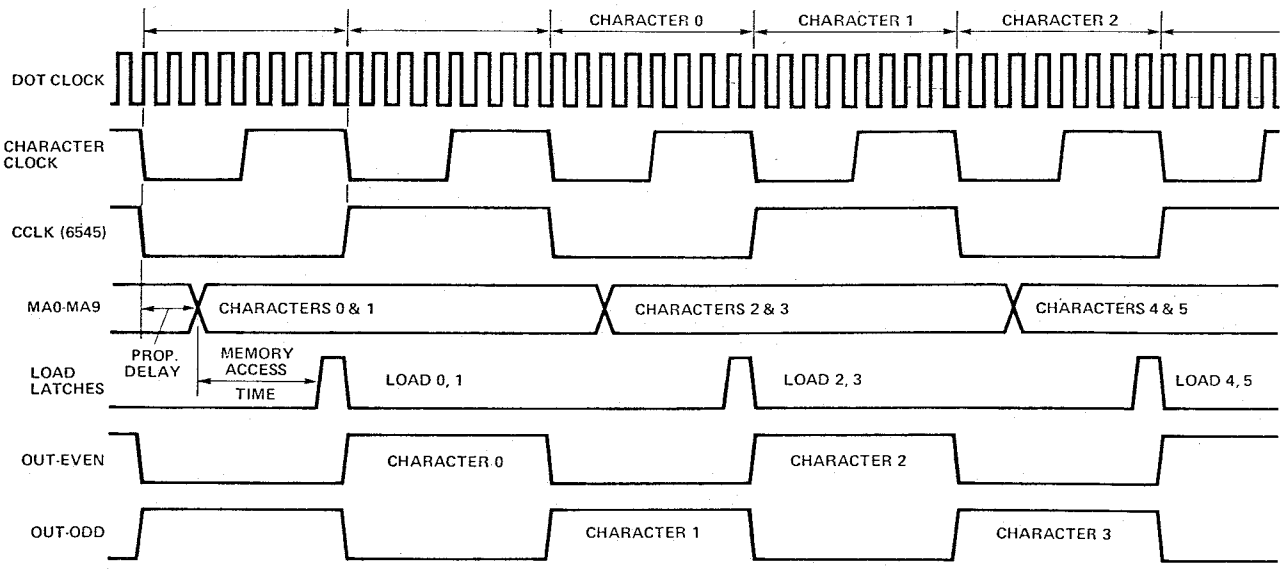

Figure 5-4. System Timings

The remaining signals shown in Figure 5-4 illustrate the approximate timing requirements for the load and output gating signals needed to operate the two 8-bit holding registers for the odd and even memory blocks. Note that the LOAD signal causes the video display memory outputs (odd and even characters) to be loaded into the latches and separate odd and even output controls alternately select the latches to drive the input lines of the character generator ROM.

Propagation delays through each functional section must be carefully accounted for. Figure 5-4 is primarily intended to demonstrate the alternating nature of the odd and even memory block timing control.

5.5 Programming Considerations

Special considerations must be made to accommodate the effects of this technique on the register programming required by the SY6545. The following registers are affected:

1. Horizontal Total.
2. Horizontal Displayed.
3. Horizontal Sync Position.
4. Horizontal/Vertical Sync Width.

In each case, the programmed value must be half the desired result. For example, to achieve 80 horizontal displayed characters per line, 40 must be programmed. Thus, it is seen that only even numbers of horizontal characters may be selected. This limitation is normally not significant, however, since standard displays require even numbers of columns.

5.7 Cursor Effect

There is one other noteworthy effect of this method. That is, the cursor output signal from the SY6545 will be two characters in duration, the odd and even character of the address selected by the cursor registers in the SY6545. To achieve a single character cursor, external logic must be incorporated.

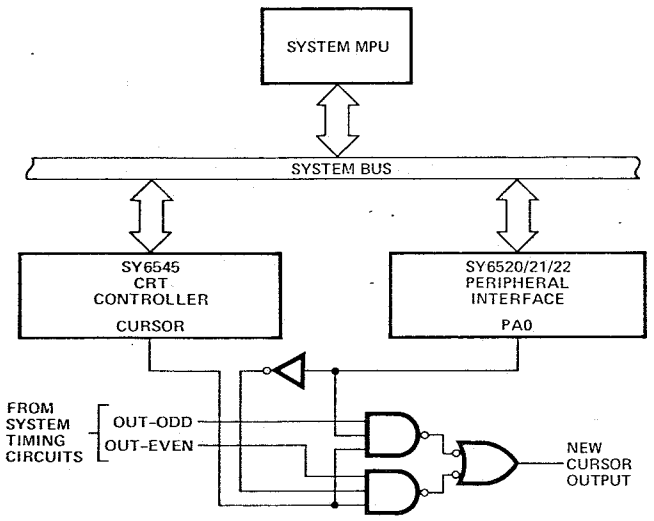

Figure 5-5. Cursor Gating Logic

A simple technique is illustrated in Figure 5-5. In this approach, the cursor output from the SY6545 is gated with either the ODD or the EVEN latch select signal (shown in Figures 5-1 and 5-4), depending on the state of the peripheral pin, PA0. Thus, when the cursor address is set in the SY6545, the PA0 bit in the peripheral interface device must be set to either a "1", to select the odd character, or a "0", for the even. Other solutions are also possible, but this one is shown for demonstration purposes.

5.8 Summary

A technique has been presented which enables the SY6545 CRT Controller to be utilized in applications requiring higher character rates than are specified for the device. This particular method effectively doubles the character rate with relatively minimal hardware and software impact. Extensions to this approach may be utilized for even faster systems, using the same basic method.

6.0 Dynamically Changing Screen Display Formats

The SY6545 CRT Controller permits fully-programmable video screen display formatting. The screen parameters which are programmable are:

- Horizontal Sync Position and Width
  - — This permits positioning the displayed text on the screen in the horizontal direction
- Vertical Sync Position and Width
  - — This permits positioning the displayed text in the vertical direction
- Horizontal Total Characters and Displayed Characters
  - — This permits selection of the number of displayed columns in each row
- Vertical Total Characters and Displayed Characters
  - — This permits selection of the number of displayed rows on the screen
- Scan Lines per Row
  - — This allows selection of the size of each displayed character — the height, including spacing

It is possible to alter these screen display parameters, within the confines of a specific hardware configuration. Care must be taken, however, to ensure that only those parameters whose alteration will still function with the hardware of the system, are allowed to change. For example, if the character clock (CCLK) rate of the system is fixed, it is important to change the display formats in a way which will not affect the overall frame rate (normally 60 Hz). Typically, for a fixed hardware design, the display formats which can be changed are:

- Horizontal Sync position
- Vertical Sync position
- Horizontal Displayed Characters

6.1 How to Change Parameters Dynamically

To change screen display formats dynamically means to re-program the SY6545 on-the-fly; that is, to re-program without disturbing the display. The SY6545 provides for

dynamically changing display formats by means of the $\overline{RES}$ pin on the device. The function of the pin is as follows (from the SY6545 data sheet).

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display timing with line frequency.

Thus, $\overline{RES}$ actually stops all counters within the SY6545. Program registers, however, are unaffected and may, in fact, be altered when $\overline{RES}$ is low. If this happens, then, when $\overline{RES}$ goes high, the display scan will start with the new display formats.

6.3 System Considerations

In a system, $\overline{RES}$ is normally used to synchronize the frame rate of the display to the 50/60 Hz line frequency, to prevent apparent flicker caused without synchronism. This can be achieved by using a zero-crossing detector and some logic on the line frequency and, from this, generating $\overline{RES}$.

From this, it is only necessary that the system processor be able to detect when $\overline{RES}$ is active (low) and to re-program the SY6545 before $\overline{RES}$ again goes high. Detection of the state of $\overline{RES}$ can be achieved by, for example, connecting it to a Peripheral Interface Adapter, like the SY6520 or SY6522. The duration of the $\overline{RES}$ signal must be adequate for the processor to sense its state and re-program the SY6545 registers. Depending on how many registers need to be re-programmed, the $\overline{RES}$ width should be anywhere from 30 μsec to 150 μsec, and can be calculated by writing the necessary program code and counting the cycles needed to execute it. A simplified system diagram is shown in Figure 6-1.

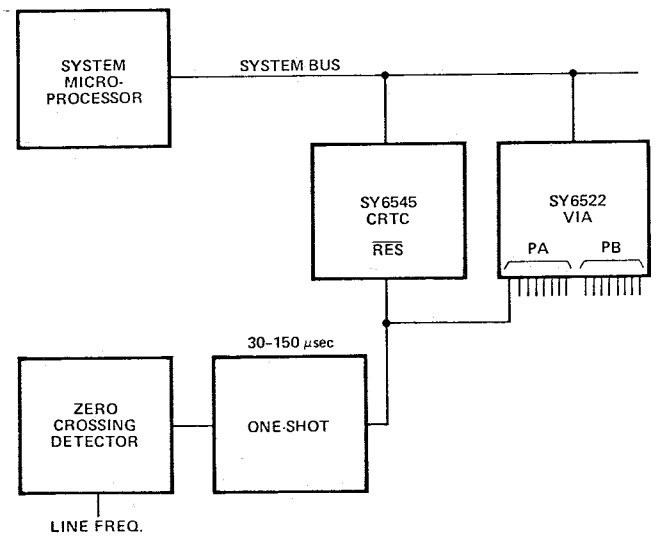

Figure 6-1. $\overline{RES}$ Used for Line Frequency Synchronism

6.4 Summary

A scheme has been presented to dynamically re-program the SY6545 screen display format by utilizing the capabilities inherent in the $\overline{RES}$ pin. Other schemes may be devised, but care must be taken to ensure an undisturbed display for optimum system design.

7.0 Using LPEN as Keyboard Scan Strobe

Much has been said and written about the impact of microprocessor technology on system design. It is clear that microprocessors not only permit existing systems to be implemented more cost-effectively, but that new systems, previously impractical, may now be very feasible and marketable. Two more recent developments extend this idea even further. They are single-chip microcomputers and dedicated controllers.

Single-chip microcomputers extend the impact of microprocessors toward the low-end of system applications. The characteristics which lend themselves more effectively to this technology are small size, low cost, relatively simple tasks, and high production volume.

The high-end of the spectrum is supported by new programmable dedicated controllers. Included in this category are devices such as floppy disk controllers. keyboard encoders, communications controllers, IEEE-488 bus controllers, DMA controllers, and interrupt controllers. In perspective, the main advantages to be gained by these devices are:

1. Low parts count for small system size.
2. Lower system cost.
3. High level of controller autonomy — microprocessor is relieved of detailed operational control
4. Flexible system design gained by programmability.
5. Inventory simplification by requiring only one device for several different system designs.

The area of CRT controllers is especially interesting. The evolution from teletype terminals to video terminals has been achieved in part by the utilization of microprocessor-based designs. The next steps in evolution will be towards even more sophistication and lower prices and will come about with the inclusion of dedicated MOS/LSI CRT controller devices into CRT system design, which already include microprocessor technology.

The wide variety of CRT controllers becoming available permits system design to be specifically tailored to the capabilities desired in the system. In some cases, clever use of the particular CRT controller can result in additional system features not foreseen when the controller was originally conceived. In this case, the CRT system can gain a competitive advantage if one or more of these capabilities is exploited. The remainder of this discussion focuses on just such a utilization, namely with the Synertek SY6545 device.

7.1 The SY6545 CRT Controller

The SY6545 is a microprocessor peripheral device intended to interface 6500/6800 microprocessors in CRT control applications. It is fully programmable, permitting a wide variety of screen display formats to be easily implemented.

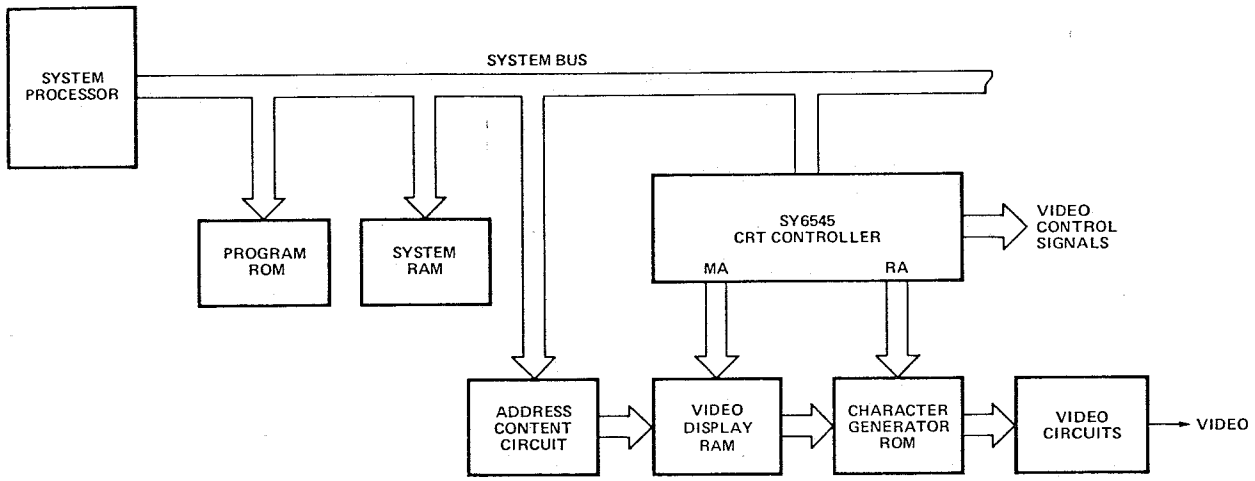

Figure 7-1. MPU-Based CRT System

Included in the SY6545 are counter outputs for memory addressing and a strobe input for light pen applications. The very nature of these pin functions allows these lines to be used as keyboard drive and sense signals, without affecting normal CRT operation. In other words, the SY6545 can be used simultaneously as a CRT Controller and a keyboard scanner. This note explains how this can be achieved.

7.2 Basic CRT Control Operation

Figure 7-1 shows a simplified block diagram of a microprocessor-based CRT Control system.

Note that the CRT Controller works in conjunction with a Video Display RAM (for screen display information storage), a character generator ROM (to generate dot patterns for each character) and video control circuits. All these components are required to keep the screen display "alive"; the data must be repetitively generated as video inputs to the CRT monitor or TV-type display. As a result, the address lines (MA0-MA13) are constantly counting from the start address (address of the first charcter to be displayed) to the end address (last character displayed). For a display size of 80 columns by 24 rows, this is 1920 characters, or a block of 1920 addresses, start to finish.

7.3 LPEN Input Strobe

The LPEN input pin on the SY6545 is intended as a strobe input for light pen applications. Internally, a signal on this pin gates the scanning counter state (MA0-MA13) into a light pen holding register. In this way, when the CRT electron beam passes across the light pen held at the surface of the video screen, a signal generated by the light pen and applied to the LPEN input to the SY6545 will effectively identify the location of the light pen, relative to the scanning addresses. In most CRT systems, there is no light pen capability required. Thus, there is very little system impact if this feature is used as a keyboard strobe, instead of its intended light pen function.

7.4 A Simple Keyboard Scanning Configuration

Figure 7-2 illustrates the hardware configuration of the SY6545 with an 8x8 crosspoint keyboard matrix.

Note that the MA lines are utilized to scan the keyboard, but that their operation with the screen display RAM is totally unaffected. Using these lines to drive the keyboard requires no special programming steps, only a 1-of-8 decoder (active-low outputs) for driving the keyboard lines and 1-of-8 data selector (active-high output) to sense the keyboard and drive the LPEN strobe pin of the SY6545. However, in this case the LPEN line is not available for light pen applications, but as indicated previously, this is not a significant drawback.

7.5 Keyboard Strobe Timing

The MA0-MA13 addresses are generated as a result of the SY6545 CCLK (character clock) input. This signal occurs once every character time and automatically increments the scan counter for the MA lines. The closure of a key will have no effect until the specific drive line is energized and the specific sense line is gated to the LPEN input. At this time, the LPEN strobe occurs and the MA0-MA13 counter

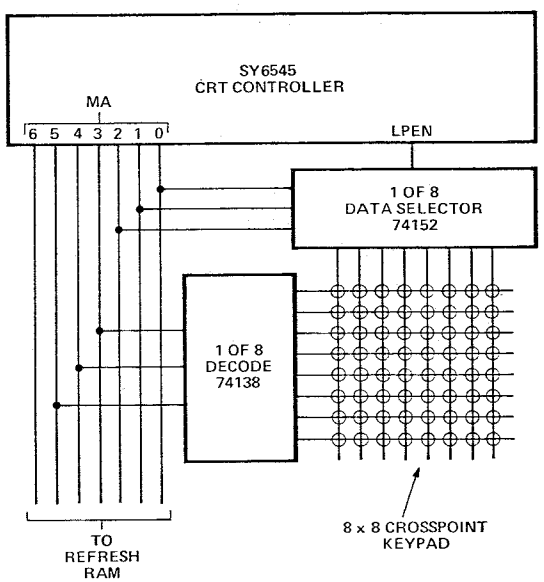

Figure 7-2. Keyboard Scan Circuits for Use with SY6545 CRTC

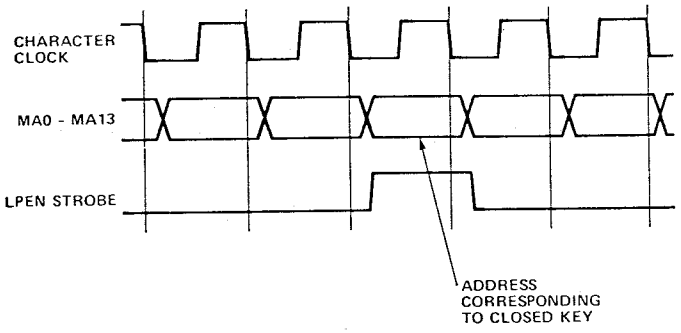

Figure 7-3. LPEN Strobe Timing for Keyboard Scan

inside the SY6545 is loaded into the LPEN holding register, also inside the SY6545. The timing is shown in Figure 7-3.

All timing is very clean and not sensitive to race conditions or transients on any signals.

7.6 Programming Considerations for Key Identification

For this example, six MA lines are used.

- MA0-MA2 identify the sense line for the key closed.
- MA3-MA5 identify the drive line of the key closed.

However, the SY6545 LPEN strobe will actually cause the next sequential address to be loaded into the internal holding register, due to internal timing skews in the SY6545. Thus, it is important to decrement the number stored into the holding register before decoding it to determine the key closed.

For example, consider the key closed as shown in Figure 7-4.

For this case, the MA lines which cause the LPEN strobe are,

7	6	5	4	3	2	1	0
–	–	1	1	0	1	0	1

DRIVE LINE 6 — SENSE LINE 5

However, the contents of the internal LPEN register will be,

7	6	5	4	3	2	1	0
–	–	1	1	0	1	1	0

This is easily corrected in the system program by decrementing after the register is read out.

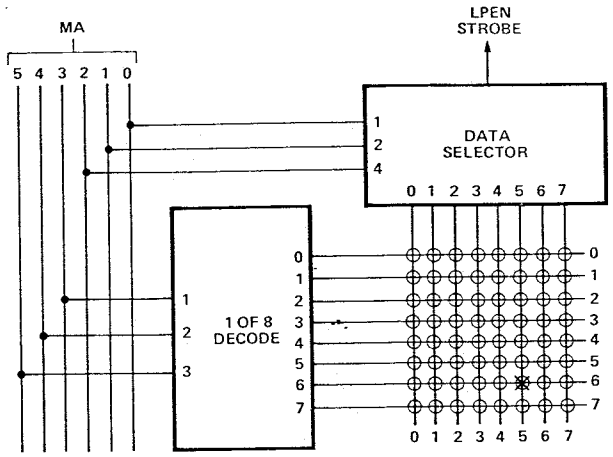

Figure 7-4. Key Closure Identification

7.7 Use of the LPEN Status Bit in the SY6545

A light pen status indication is available in the SY6545 to identify that a strobe has occurred. This is used by the system processor as a means of determining that a key has been pressed and the LPEN register may be interrogated. This status bit is not usable with the interrupt facility of the microprocessor, so the processor must periodically scan the status register to check for key closure. This can be done either by hardware timers to initiate the processor status check or simply by programming periodic checks to occur.

7.8 De-Bounce Considerations

Key de-bounce must be handled by software, as well. Once a key is determined to be down, several iterations of checking the LPEN status bit and holding register must be made to verify that it is indeed down, and not simply caused by system noise. Likewise, key release must be determined over several iterations, as well.